CLAIMS

What is claimed is:

1. A programmable logic device comprising:

circuit regions including region input multiplexers to select signals for routing to the circuit regions;

routing resources including routing resources coupled to the region input multiplexers and including a first routing line coupled to route signals between the circuit regions, the first routing line including a first driver input multiplexer ("DIM") to select signals for driving the first routing line; and

one or more connection lines coupling respective outputs of one or more of the region input multiplexers to the first DIM.

2. The programmable logic device of claim 1 wherein the first routing line is a longer line than at least some of the other routing resources.

3. The programmable logic device of claim 1 wherein the connection lines are coupled to the region input multiplexer outputs through programmable connections.

4. The programmable logic device of claim 1 wherein the circuit regions include logic array blocks.

5. The programmable logic device of claim 1 wherein the circuit regions include dedicated blocks.

6. The programmable logic device of claim 1 wherein:

the routing resources also include a second routing line coupled to route signals between the circuit regions, the second routing line including a second driver input multiplexer ("DIM") to select signals for driving the second routing line; and

the programmable logic device further comprises one or more connection lines coupling respective outputs of one or more of the region input multiplexers to the second DIM.

7. The programmable logic device of claim 6 wherein the first routing line is oriented in a direction that is the same as an orientation direction of the second routing line.

8. The programmable logic device of claim 6 wherein the first routing line is oriented in a direction different than an orientation direction of the second routing line.

9. The programmable logic device of claim 6 wherein the first and second routing lines are longer lines than at least some of the other routing resources.

10. A data processing system comprising the programmable logic device of claim 1.

11. A method of routing signals from a routing resource to a destination routing resource of a programmable logic device, the programmable logic device including circuit regions, the method comprising:

routing the signals from the routing resource to the destination routing resource through a region input multiplexer.

12. The method of claim 11 wherein the signals are routed to the destination routing resource through an input multiplexer ("DIM") of the second routing resource.

13. The method of claim 11 wherein the destination routing resource is longer than other similarly oriented routing resources in a core of the programmable logic device.

14. The method of claim 11 wherein the region input multiplexer is a logic array block input multiplexer.

15. The method of claim 11 wherein the region input multiplexer is a dedicated block input multiplexer.

16. A programmable logic device comprising:

core routing means for routing signals between circuit regions;

circuit region input means for routing signals to a circuit region; and

means for routing signals from one of the core routing means to another through the circuit region input means.

17. A programmable logic device comprising:

circuit regions including sub-regions, the sub-regions including sub-region input multiplexers coupled to select signals for routing to the sub-regions;

routing resources including routing resources coupled to the sub-region input multiplexers and including a first routing line coupled to route signals between the circuit regions, the first routing line including a first driver input multiplexer ("DIM") to select signals for driving the first routing line; and

one or more connection lines coupling respective outputs of one or more of the sub-region input multiplexers to the first DIM.

18. The programmable logic device of claim 17 wherein the first routing line is a longer line than at least some of the other routing resources.

19. The programmable logic device of claim 17 wherein the connection lines are coupled to the outputs of the sub-region input multiplexers through programmable connections.

20. The programmable logic device of claim 17 wherein the routing resources are coupled to the sub-region input multiplexers through region input multiplexers.

21. The programmable logic device of claim 20 further comprising one or more connection lines coupling respective outputs of one or more of the region input multiplexers to the first DIM.

22. The programmable logic device of claim 20 wherein:

the routing resources also include a second routing line coupled to route signals between the circuit regions, the second routing line including a second input multiplexer ("DIM") to select signals for driving the second routing line; and

the programmable logic device further comprises one or more connection lines coupling respective outputs of one or more of the region input multiplexers to the second DIM.

23. The programmable logic device of claim 17 wherein the regions include logic array blocks and the sub-regions include logic elements.

24. The programmable logic device of claim 17 wherein the regions include dedicated blocks.

25. The programmable logic device of claim 17 wherein:

the routing resources also include a second routing line coupled to route signals between the circuit regions, the second routing line including a second input multiplexer ("DIM") to select signals for driving the second routing line; and

the programmable logic device further comprises one or more connection lines coupling respective outputs of one or more of the sub-region input multiplexers to the second DIM.

26. The programmable logic device of claim 25 wherein the first routing line is oriented in a direction that is the same as an orientation direction of the second routing line.

27. The programmable logic device of claim 25 wherein the first routing line is oriented in a direction different than an orientation direction of the second routing line.

28. The programmable logic device of claim 25 wherein the first and second routing lines are longer lines that at least some of the other routing resources.

29. A data processing system comprising the programmable logic device of claim 17.

30. A method of routing signals from a routing resource to a destination routing resource of a programmable logic device, the programmable logic device including circuit regions and sub-regions, the method comprising:

routing the signals from the routing resource to the destination routing resource through a sub-region input multiplexer.

31. The method of claim 30 wherein the signals are routed from the routing resource to the sub-region input multiplexer through a region input multiplexer.

32. The method of claim 31 wherein the sub-region input multiplexer is coupled to a secondary signal generator of a logic region of the programmable logic device.

33. The method of claim 30 wherein the signals are routed to the second routing resource through an input multiplexer ("DIM") of the second routing resource.

34. A programmable logic device including circuit regions and sub-regions, the programmable logic device comprising:

core routing means for routing signals between circuit regions;

sub-region input means for routing signals to sub-regions; and

means for routing signals from one of the core routing means to another through the sub-region input means.

35. The programmable logic device of claim 34 further comprising region input means for routing signals to the regions, the region input means being coupled on a signal path between the one of the core routing means and the other of the core routing means.

36. The programmable logic device of claim 34 wherein the region input means is coupled on a signal path between the one of the core routing means and the sub-region input means.